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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,885	12/21/2001	Youfeng Wu	42390P12634	2294

7590 09/23/2004

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EXAMINER	
PHAM, CHRYSTINE	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/028,885	WU ET AL.
	Examiner	Art Unit
	Chrystine Pham	2122

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 5-8, 12-15, and 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Santhanam (US 5704053), hereinafter, *Santhanam*.

As per claim 1, *Santhanam* teaches a system (e.g., see FIGS.1, 2 & associated text), a computer-readable medium storing executable instructions (e.g., see *memory 13, cache 12* FIG.1 & associated text, see FIG.2 & associated text), and method for:

- an analyzing module (e.g., see *200* FIG.11 & associated text) for analyzing/determining a stride profile (e.g., col.16:26-30), and
- an optimizing module (e.g., see *LL0 24* FIG.8 & associated text) for inserting a prefetch instruction (e.g., col.5:17-21) immediately before a load instruction using stride profiling information (e.g., col.23:5-10).

As per claim 5, *Santhanam* teaches the method of claim 1, further comprising the step of the optimizing module analyzing a range of cache area accessed by a load (e.g., col.6:22-24, see FIG.4 & associated text, col.12:12-16) in a loop (e.g., see FIG.3 & associated text), and inserting a prefetch instruction at the additive combination of a load address P and a determined compile time constant (e.g., col.12:18-43).

As per claim 6, *Santhanam* teaches the method of claim 5, further comprising the step of the optimizing module determining a prefetching distance (e.g., see *93* FIG.9 & associated text)

from at least one of a cache profile and a compiler analysis (e.g., col.10:12-14, see *LLO 24* FIG.8 & associated text).

As per claim 7, *Santhanam* teaches the method of claim 1, further comprising the analyzing module determining a cache profile (e.g., col.5:30-31) to assist in determining appropriate insertion of a prefetch instruction (i.e., provide information to the optimizing module) (e.g., col.3:47-55, col.3:66-col.4:2, col.6:6-8, col.7:59-col.8:7, col.8:30-35, col.10:12-14).

Claim 8 recites a computer-readable medium version of the method addressed in claim 1, therefore, is rejected for the same reasons as cited in claim 1.

As per claims 12-14, they recite limitations which have been addressed in claims 5-7, therefore, are rejected for the same reasons as cited in claims 5-7.

Claim 15 recites a system version of the method addressed in claim 1, therefore, is rejected for the same reasons as cited in claim 1.

As per claims 19-21, they recite limitations which have been addressed in claims 5-7, therefore, are rejected for the same reasons as cited in claims 5-7.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-3, 9-10, 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Santhanam* as applied to claims 1, 8 and 15 above further in view of Grimsrud (US 5726913), hereinafter, *Grimsrud*.

As per claim 2, *Santhanam* teaches the method of claim 1, further comprising the steps of executing the instrumented program (e.g., col.2:54-55, col.4:60-64, col.8:26-29), and a stride profiling module collecting a stride profile analysis (e.g., see Abstract), identifying candidate loads (e.g., see FIG.3 & associated text, col.6:41-43, col.7:11-13), grouping candidate loads (e.g., see FIG.11 & associated text, col.16:28-30). *Santhanam* does not expressly disclose grouping selected profiled loads, inserting profiling instructions. However, *Grimsrud* discloses system (e.g., see FIGS.1, 2 & associated text) and method for selecting profiled loads (e.g., see *102* FIG.5 & associated text) and generating profiling instructions (e.g., see *104,108, 110* FIG.5 & associated text, see FIG.7 & associated text) which comprises collecting and providing to a top stride/differential profile (e.g., see *Locality Characteristic Profiles 72a* FIG.2 & associated text) top N most frequently occurring stride values (e.g., see *stride 1* FIG.9a & associated text) and frequencies (e.g., see *5/7* FIG.9a & associated text, see *110* FIG.5 & associated text), top M most frequently occurred differences (e.g., see *distance 3-4* FIG.9a & associated text) of successive strides (e.g., see *strides –2 to 6* FIG.9a & associated text) and their frequencies (e.g., see third row "*2/7, 1/7, 3/7, 1/7*" FIG.9a & associated text, col.4:30-33). It would have been obvious to one of ordinary skill in the pertinent art at the time the invention was made to modify the teaching of *Santhanam* with that of *Grimsrud* to obtain the profiling instructions for insertion. And the motivation for doing so would have been that the profiling instructions (i.e., stride values/differences and their frequencies) provide locality characteristics for different load instructions/memory accesses, hence, enabling interactions between workloads and locality dependent subsystems to be analyzed for high propensity of activities. Furthermore, profiling instructions can be used to generate expected performance indices for various workload and locality dependent subsystem combinations.

As per claims 3, 9-10 and 16-17, they recite limitations which have been addressed in claim 2, therefore, are rejected for the same reasons as cited in claim 2.

5. Claims 4, 11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Santhanam* in view of *Grimsrud* further in view of Mirza et al. (US 5357618), hereinafter, *Mirza et al.*.

As per claim 4, the combined teaching of *Santhanam* and *Grimsrud* (hereinafter ***S2***) teach the method of claim 2, comprising the step of profiling the difference of successive strides to collect the top M most frequently occurred differences and their frequencies to provide a top differential profile (see claim 2). ***S2*** do not expressly disclose distinguishing phased stride sequences from alternated stride sequences. However, *Mirza et al.* disclose a method (e.g., see Abstract) and system (e.g., see FIG.1 & associated text) for distinguishing phased stride sequences (e.g., see *30, 40* FIG.5 & associated text, col.2:56-63, col.7:32-34) from alternated stride sequences (e.g., col.3:5-7, col.5:4-10, col.8:3-6, col.8:28-36, col.8:40-46). It would have been obvious to one of ordinary skill in the pertinent art at the time the invention was made to modify the teaching of ***S2*** to include distinguishing between phased and alternated stride sequences. And the motivation for doing so would have been to inhibit unnecessary prefetching of data (i.e., when there is no stride pattern, or when stride pattern is broken) to reduce memory and switch demand while diminishing cache pollution which allows high-reuse data to remain in the cache.

As per claims 11 and 18, they recite limitations which have been addressed in claim 4, therefore, are rejected for the same reasons as cited in claim 4.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Optimizing compiler having data cache prefetch spreading, Hsu, Wei et al. (US 5854934)
- Stride-based data address prediction structure Pickett, James K. (US 5854921)
- Method of prefetching data for references with multiple stride directions Gornish, Edward H. et al. (US 5752037)
- Memory pattern analysis tool for use in optimizing computer program code Chang, Po-hua (US 5805863)
- Microprocessor circuits, systems, and methods implementing a loop and/or stride predicting load target buffer Cai, George Z. N. et al. (US 5953512)
- Global stride prefetching apparatus and method for a high-performance processor Spillinger, Illan Y. (US 6055622)
- Updating data dependencies for loop strip mining Caracuzzo, Terry J. (US 6059841)
- Microprocessor circuits, systems, and methods implementing a load target buffer with entries relating to prefetch desirability Cai, George Z. N. et al. (US 6216219)
- Method of operating a computer system by identifying source code computational elements in main memory McCarthy, Dominic Paul et al. (US 6336154)
- Memory access optimizing method Motokawa, Keiko et al. (US 6401187)
- Data processor Van Der Wolf, Pieter et al. (US 6415377)
- Integration of data prefetching and modulo scheduling using postpass prefetch insertion Tirumalai, Partha Pal et al. (US 6634024)
- Insertion of prefetch instructions into computer program code Pieper, John Samuel et al. (US 6675374)

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chrystine Pham whose telephone number is 703.605.1219. The examiner can normally be reached on Mon-Fri, 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q Dam can be reached on 703.305.4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chrystine Pham
Examiner
GAU 2122

***After October 25, 2004, examiner can be reached at new telephone number (571) 272-3702, and the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3694.

TUAN DAM
SUPERVISORY PATENT EXAMINER